Total No. of Questions : 18

Total No. of Pages : 02

B.Tech.(CSE) (2018 Batch) (Sem.-4) COMPUTER ORGANIZATION AND ARCHITECTURE Subject Code : BTES-401-18

M.Code : 77627

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

- 1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
- 2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
- 3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

SECTION-A

Write briefly :

- 1. Distinguish between auto increment and auto decrement mode.
- 2. Write a register transfer sequence to read a word from memory.
- 3. Mention some advantages
- 4. How many memory chips are needed to construct 2M*16 memory system using 512K*8 static memory chips
- 5. Define and explain memory hierarchy.
- 6. What is a Micro Program Sequencer?
- 7. State the advantages of Virtual Memory.
- 8. Write the logic equations of binary half adder?
- 9. Under what situations the micro program counter is not incremented after a new instruction is fetched from micro program memory.
- 10. What are the disadvantages of increasing the number of stages in pipeline processing?

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SECTION-B

- 11. Explain briefly Integer Addition and Subtraction Algorithm.
- 12. What is a Mapping Function? What are the ways cache can be mapped?
- 13. Explain the working of carry look ahead adder.
- 14. With examples explain the data transfer, Logic and Program control instructions.
- 15. Explain in detail about the Flynn's classification.

SECTION-C

- 16. What is Instruction Hazard? Explain the methods of dealing with instruction hazards.
- 17. Explain the basic organization of micro programmed control unit and generation of control signals using micro program.
- 18. Discuss about the various components of computer system.

NOTE : Disclosure of Identity by writing Mobile No. or Marking of passing request on any paper of Answer Sheet will lead to UMC against the Student.

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